H1938

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 May 2004 (27.05.2004)

PCT

(10) International Publication Number
WO 2004/044992 A1

(51) International Patent Classification[7]: H01L 29/786, 29/423, 21/336

(21) International Application Number: PCT/US2003/032662

(22) International Filing Date: 14 October 2003 (14.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/290,158 8 November 2002 (08.11.2002) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Snunyvale, CA 94088-3453 (US).

(72) Inventors: AHMED, Shibly, S.; 350 Elan Village Lane, #105, San Jose, CA 95134 (US). WANG, Haihong; 34170 Donahue Terrace, Fremont, CA 94555 (US). YU, Bin; 1373 Poppy Way, Cupertino, CA 95014 (US).

(74) Agent: COLLOPY, Daniel, R.; Advanced Micro Devices, Inc., One AMD Place, Mail Spop 68, Sunnyvale, CA 94088-3453 (US).

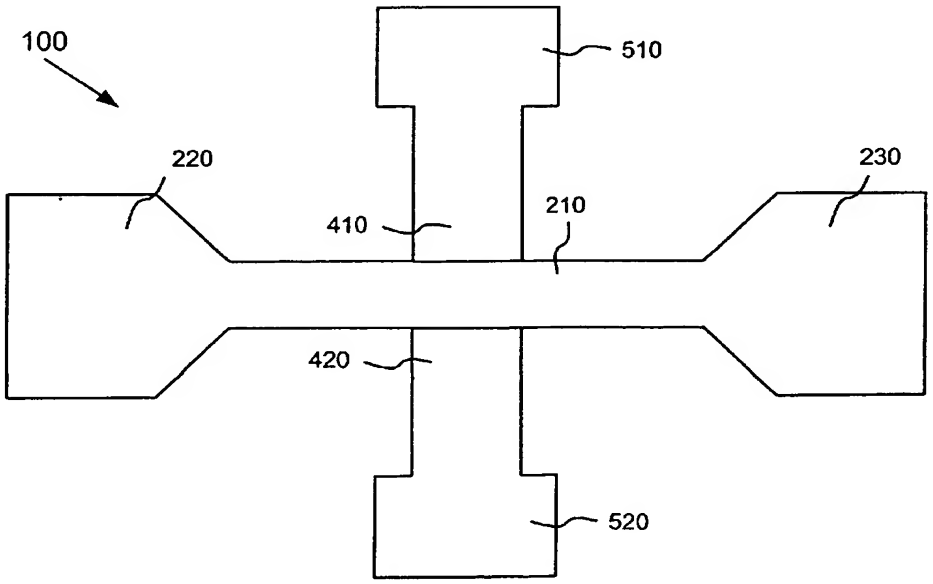
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

[Continued on next page]

(54) Title: DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES



(57) Abstract: A semiconductor device (100) may include a substrate (110) and an insulating layer (120) formed on the substrate (110). A fin (210) may be formed on the insulating layer (120) and may include a number of side surfaces and a top surface. A first gate (410) may be formed on the insulating layer (120) proximate to one of the number of side surfaces of the fin (210). A second gate (420) and may be formed on the insulating layer (120) separate from the first gate (410) and proximate to another one of number of side surfaces of the fin (210).

WO 2004/044992 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES

TECHNICAL FIELD

The present invention relates to semiconductor devices and methods of manufacturing semiconductor devices. The present invention has particular applicability to double-gate devices.

BACKGROUND ART

The escalating requirements for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In several respects, the double-gate MOSFETs offer better characteristics than the conventional bulk silicon MOSFETs. These improvements arise because the double-gate MOSFET has a gate electrode on both sides of the channel, rather than only on one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate, resulting in a stronger switching signal.

A FinFET is a recent double-gate structure that exhibits good short channel behavior. Although conventional FinFETs are referred to as "double-gate" MOSFETs, the two gates typically are physically and electrically connected and thus form a single logically addressable gate. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

Implementations consistent with the present invention provide a FinFET device with two gates that are effectively separated from each other by a conductive fin. The gates may be independently biased for increased circuit design flexibility.

Additional advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

According to the present invention, the foregoing and other advantages are achieved in part by a

semiconductor device including a substrate and an insulating layer formed on the substrate. A fin may be formed on the insulating layer and may include a number of side surfaces and a top surface. A first gate may be formed on the insulating layer proximate to one of number of side surfaces of the fin. A second gate may be formed on the insulating layer separate from the first gate and proximate to another one of number of side surfaces of the fin.

According to another aspect of the invention, a method of manufacturing a semiconductor device may include forming an insulating layer on a substrate and forming a fin structure on the insulating layer. The fin structure includes a first side surface, a second side surface, and a top surface. The method may also include forming source and drain regions at ends of the fin structure and depositing a gate material over the fin structure. The gate material surrounds the top surface and the first and second side surfaces. The gate material may be etched to form a first gate electrode and a second gate electrode on opposite sides of the fin. The deposited gate material may be planarized proximate to the fin.

According to a further aspect of the invention a semiconductor device may include a substrate and an insulating layer formed on the substrate. A conductive fin may be formed on the insulating layer, and gate dielectric layers may be formed on side surfaces of the conductive fin. A first gate electrode may be formed on the insulating layer. The first gate electrode may be disposed on a first side of the conductive fin adjacent to one of the gate dielectric layers. A second gate electrode may be formed on the insulating layer. The second gate electrode may be disposed on an opposite side of the conductive fin adjacent to another one of the gate dielectric layers and spaced apart from the first gate electrode.

Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

Fig. 1 is a cross-section illustrating exemplary layers that may be used for forming a fin in accordance with an embodiment of the present invention.

Fig. 2A schematically illustrates the top view of a fin structure in accordance with an exemplary embodiment of the present invention.

Fig. 2B is a cross-section illustrating the fin structure of Fig. 2A in accordance with an exemplary embodiment of the present invention.

Fig. 3 is a cross-section illustrating the formation of a gate dielectric layer and gate material on the device of Fig. 2B in accordance with an exemplary embodiment of the present invention.

Fig. 4 is a cross-section illustrating the planarizing of the gate material of Fig. 3 in accordance with an exemplary embodiment of the present invention.

Fig. 5 schematically illustrates the top view of the semiconductor device of Fig. 4 in accordance with an exemplary embodiment of the present invention.

Figs. 6A-6D are cross-sections illustrating the induction of tensile strain in a fin in accordance with another implementation of the present invention.

Figs. 7A-7F are top and cross-sectional views illustrating formation of a fully silicided gate in a FinFET in accordance with another implementation of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

Implementations consistent with the present invention provide double gate FinFET devices and methods of manufacturing such devices. The gates in the FinFET devices formed in accordance with the present invention are effectively separated from each other and may be separately biased.

Fig. 1 illustrates the cross-section of a semiconductor device 100 formed in accordance with an embodiment of the present invention. Referring to Fig. 1, semiconductor device 100 may include a silicon on insulator (SOI) structure that includes a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 on the buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1000 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 300 Å to about 1500 Å. Silicon layer 130 is used to form a fin structure for a double gate transistor device, as described in more detail below.

In alternative implementations consistent with the present invention, substrate 110 and layer 130 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

A dielectric layer 140, such as a silicon nitride layer or a silicon oxide layer (e.g., SiO_2), may be formed over silicon layer 130 to act as a protective cap during subsequent etching processes. In an exemplary implementation, dielectric layer 140 may be deposited at a thickness ranging from about 150 Å to about 600 Å. Next, a photoresist material may be deposited and patterned to form a photoresist mask 150 for subsequent processing. The photoresist may be deposited and patterned in any conventional manner.

Semiconductor device 100 may then be etched and the photoresist mask 150 may be removed. In an exemplary implementation, silicon layer 130 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120 to form a fin. After the formation of the fin, source and drain regions may be formed adjacent the respective ends of the fin. For example, in an exemplary embodiment, a layer of silicon, germanium or combination of silicon and germanium may be deposited, patterned and etched in a

conventional manner to form source and drain regions.

Fig. 2A schematically illustrates the top view of a fin structure on semiconductor 100 formed in such a manner. Source region 220 and drain region 230 may be formed adjacent the ends of fin 210 on buried oxide layer 120, according to an exemplary embodiment of the present invention.

Fig. 2B is a cross-section along line A-A' in Fig. 2A illustrating the fin structure in accordance with an exemplary embodiment of the present invention. Dielectric layer 140 and silicon layer 130 have been etched to form fin 210. Fin 210 may include silicon 130 and a dielectric cap 140.

Fig. 3 is a cross-section illustrating the formation of a gate dielectric layer and gate material on fin 210 in accordance with an exemplary embodiment of the present invention. A dielectric layer may be formed on fin 210. For example, a thin oxide film 310 may be thermally grown on fin 210, as illustrated in Fig. 4. The oxide film 310 may be grown to a thickness of about 10 Å to about 50 Å and may be formed on the exposed side surfaces of silicon 130 in fin 210 to act as a dielectric layer for a subsequently formed gate electrode. Similar to the oxide film 310, the dielectric cap 140 may provide electrical insulation for the top surface of fin 210.

A gate material layer 320 may be deposited over semiconductor device 100 after formation of the oxide film 310. The gate material layer 320 may comprise the material for the subsequently formed gate electrode. In an exemplary implementation, the gate material layer 320 may include polysilicon deposited using conventional chemical vapor deposition (CVD) to a thickness ranging from about 300 Å to about 1500 Å. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material.

Two gates may be defined in the gate material layer 320 by lithography (e.g., photolithography). Gate material layer 320 may be selectively etched to form a gate structure out of the gate material layer 320 on device 100. Forming the gate structure in such a manner may leave some gate material 320 on top of the dielectric cap 140, for example as illustrated in Fig. 3.

Fig. 4 is a cross-section illustrating the planarizing of the gate material 320 in accordance with an exemplary embodiment of the present invention. Excess gate material may be removed (e.g., from above the dielectric cap 140) to planarize the fin region of the semiconductor device 100. For example, chemical-mechanical polishing (CMP) may be performed so that the gate material (i.e., layer 320) is even with or nearly even with dielectric cap 140 in the vertical direction, as illustrated in Fig. 4.

Referring to Fig. 4, the gate material layer 320 in the channel region of semiconductor device 100 abuts fin 210 on the two side surfaces to form a first gate 410 and a second gate 420. The top surface of fin 210, however, is covered by dielectric cap 140. This structure is also shown in Fig. 5, which illustrates a top view of semiconductor device 100 consistent with the present invention. In Fig. 5, first gate 410 and second gate 420 are shown adjacent, but not covering, fin 210.

The gate material layer 320 may then be patterned and etched to form two gate electrodes. As illustrated in Fig. 5, semiconductor device 100 includes a double gate structure with gate electrodes 510 and 520. Gate electrodes 510 and 520 are effectively separated by fin 210 and may be separately biased, as

discussed in more detail below. The gate dielectric 310 (Fig. 4) surrounding the side surfaces of fin 210 is not shown in Fig. 5 for simplicity.

The source/drain regions 220 and 230 may then be doped. For example, n-type or p-type impurities may be implanted in source/drain regions 220 and 230. The particular implantation dosages and energies may be selected based on the particular end device requirements. One or ordinary skill in this art would be able to optimize the source/drain implantation process based on the circuit requirements and such steps are not disclosed herein in order not to unduly obscure the thrust of the present invention. In addition, sidewall spacers (not shown) may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate the source/drain regions 220 and 230.

As illustrated in Fig. 5, gate electrode 510 and gate electrode 520 are physically and electrically separated from each other. In accordance with an exemplary embodiment of the present invention, each of the gate electrodes 510 and 520 may be separately biased with different voltages when used in a circuit. The capability for independently biasing the gates 410 and 420 (via gate electrodes 510 and 520) increases the flexibility of circuit design using semiconductor device 100.

The resulting semiconductor device 100 illustrated in Fig. 5 is a double gate device with a first gate 410 and a second gate 420. The gate material layer 320 (Figs. 3 and 4) abuts two surfaces of fin 210 and provides semiconductor device 100 with increased channel width per device, as compared to a conventional double gate device. The fin 210 may also retain the dielectric cap 140 that protects the fin 210 during gate etching.

The gates 410 and 420 are also effectively separated by fin 210 and may be separately biased (via respective gate electrodes 510 and 520) based on the particular circuit requirements of device 100. This separate double gate structure provides increased flexibility during circuit design, as opposed to conventional FinFETs which include a single gat connection.

Thus, in accordance with the present invention, a double-gate FinFET device is formed with two separate gates in the channel region of the device. Advantageously, the resulting structure exhibits good short channel behavior. In addition, the present invention provides increased flexibility and can be easily integrated into conventional processing.

OTHER IMPLEMENTATIONS

In some implementations, it may be desirable to induce tensile strain in the fin of a FinFET. Figs. 6A-6D are cross-sections illustrating the induction of tensile strain in a fin in accordance with another implementation of the present invention. Fig. 6A illustrates the cross-section of a semiconductor device 600. Referring to Fig. 6A, device 600 may include a buried oxide (BOX) layer 610, a fin 620, and an SiO_2 cap 630. Elements 610-630 may be formed as described above with respect to Figs. 1-2B. Fin 620 may include silicon, germanium or a combination of silicon and germanium.

A thick sacrificial oxide layer 640 may be thermally grown on fin 620 as shown in Fig. 6B. Growing the thick (e.g., 200-400 Å) sacrificial oxide layer 640 may induce a tensile strain in fin 620. The

sacrificial oxide layer 640 may then be removed, and a thin gate oxide layer 650 may be grown, as illustrated in Fig. 6C. Gate material 660 may then be deposited over the fin 620 as shown in Fig. 6D. A FinFET may be formed from the structure in Fig. 6D in a typical manner. The fin 620 in such a FinFET will have a tensile strain, imparting qualities to the fin 620 that will be understood by those skilled in the art.

In other implementations, a FinFET with a fully silicided gate may be desired. Such a FinFET may have an incorporated metal gate that removes a polysilicon depletion effect and helps to achieve a proper threshold voltage for the FinFET. Figs. 7A and 7B are views illustrating exemplary processing for forming a FinFET with a fully silicided gate. Referring to Fig. 7A, device 700 includes a fin 710, source region 720, and drain region 730. These layers/structures may be formed as described above with respect to Figs. 1-2B. As shown in Fig. 7B, fin 710 may include a top oxide cap 740 and gate oxide 750 surrounding a silicon structure. Fin 710 may be formed on a buried oxide (BOX) layer 705.

A thin polysilicon layer 760 may be deposited on the fin 710, as shown in Fig. 7C. Then a thick bottom antireflective (BARC) layer 770 may be deposited, as shown in Fig. 7D. The gate region and contacts 780 may then be patterned and etched as shown from the top in Fig. 7E.

Source and drain regions 720 and 730 may be implanted with ions without removing the BARC layer 770. Thus, the dopants used will be stopped by the BARC layer 770 from penetrating into the channel (e.g., fin 710).

BARC layer 770 may be removed, and the polysilicon 760 is fully silicided to form a metal gate 780, as illustrated in Figs. 7E and 7F. The gate material 710 may also be planarized in a manner similar to that described above with respect to Fig. 4.

In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of CVD processes, including low pressure CVD (LPCVD) and enhanced CVD (ECVD) can be employed.

The present invention is applicable in the manufacturing of double-gate semiconductor devices and particularly in FinFET devices with design features of 100 nm and below. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various

other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

WHAT IS CLAIMED IS:

1. A semiconductor device (100), comprising:

a substrate (110);

an insulating layer (120) formed on the substrate (110);

a fin (210) formed on the insulating layer (120) and including a plurality of side surfaces and a top surface;

a first gate (410) formed on the insulating layer (120) proximate to one of plurality of side surfaces of the fin (210); and

a second gate (420) formed on the insulating layer (120) separate from the first gate (410) and proximate to another one of plurality of side surfaces of the fin (210).

2. The semiconductor device (100) of claim 1 wherein the second gate (420) is formed at an opposite side of the fin (210) from the first gate (410).

3. The semiconductor device (100) of claim 2, wherein the first and second gates (410, 420) respectively include first and second gate contacts (510, 520).

4. The semiconductor device (100) of claim 1, further comprising:

a plurality of dielectric layers (310) respectively formed along the plurality of side surfaces of the fin (210), wherein the first and second gates (410, 420) respectively abut different ones of the plurality of dielectric layers (310).

5. The semiconductor device (100) of claim 1, further comprising:

a dielectric layer (140) comprising at least one of a nitride and an oxide formed over the top surface of the fin (210, wherein a top surface of the dielectric layer (140), a top surface of the first gate (410), and a top surface of the second gate (420) are substantially coplanar.

6. A method of manufacturing a semiconductor device (100), comprising:

providing an insulating layer (120) on a substrate (110);

forming a fin structure (210) on the insulating layer (120), the fin structure (210) including a first side surface, a second side surface, and a top surface;

forming source and drain regions (220, 230) at ends of the fin structure (210);

depositing a gate material (320) over the fin structure (210), the gate material (310) surrounding the top surface and the first and second side surfaces;

etching the gate material (320) to form a first gate electrode (410) and a second gate electrode (420) on opposite sides of the fin (210); and

planarizing the deposited gate material (320) proximate to the fin.

7. The method of claim 6, further comprising:

forming a dielectric layer (140) over the top surface of the fin structure (210), wherein the planarizing includes:

polishing the gate material (320) so that no gate material (320) remains above the dielectric layer (140).

8. A semiconductor device (100), including a substrate (110), an insulating layer (120) formed on the substrate (110), a conductive fin (210) formed on the insulating layer (120), gate dielectric layers (310) formed on side surfaces of the conductive fin (210), and a first gate electrode (410) formed on the insulating layer (120), the first gate electrode (410) disposed on a first side of the conductive fin (210) adjacent one of the gate dielectric layers (310), characterized in that:

a second gate electrode (410) is formed on the insulating layer (120), the second gate electrode (420) disposed on an opposite side of the conductive fin (210) adjacent another one of the gate dielectric layers (310) and spaced apart from the first gate electrode (410).

9. The semiconductor device (100) of claim 8, further comprising:

a dielectric cap (140) formed over a top surface of the conductive fin (210), wherein neither of the first gate electrode (410) and the second gate electrode (420) extend over the dielectric cap (140).

10. The semiconductor device (100) of claim 9, wherein top surfaces of the first gate electrode (410) , the second gate electrode (420), and the dielectric cap (140) are substantially coplanar.

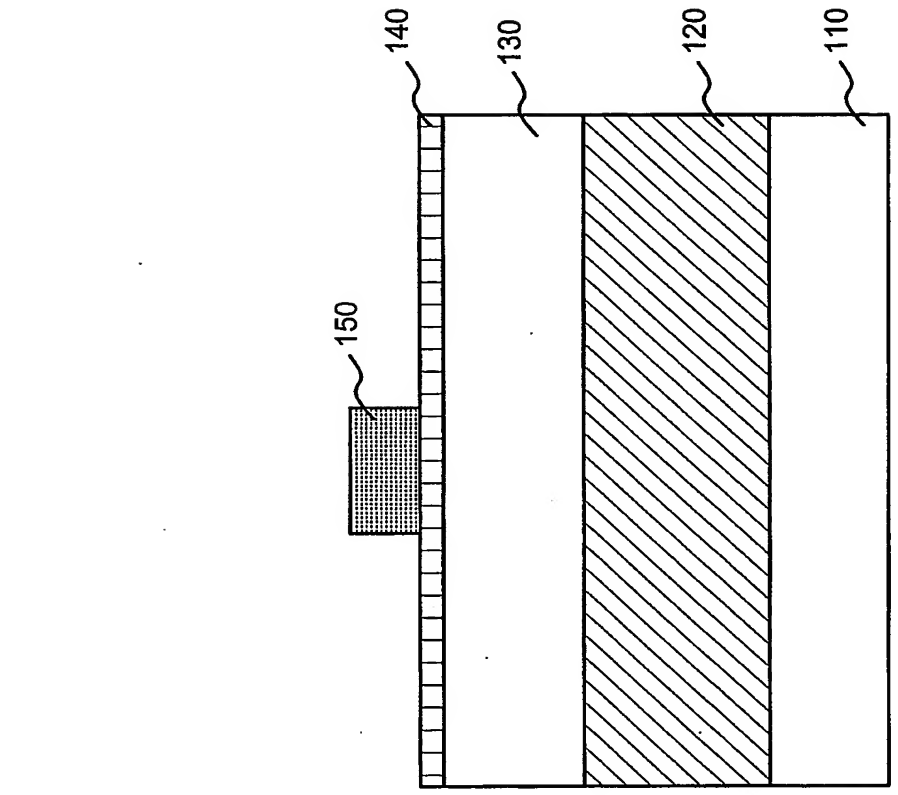


Fig. 1

Fig. 2A

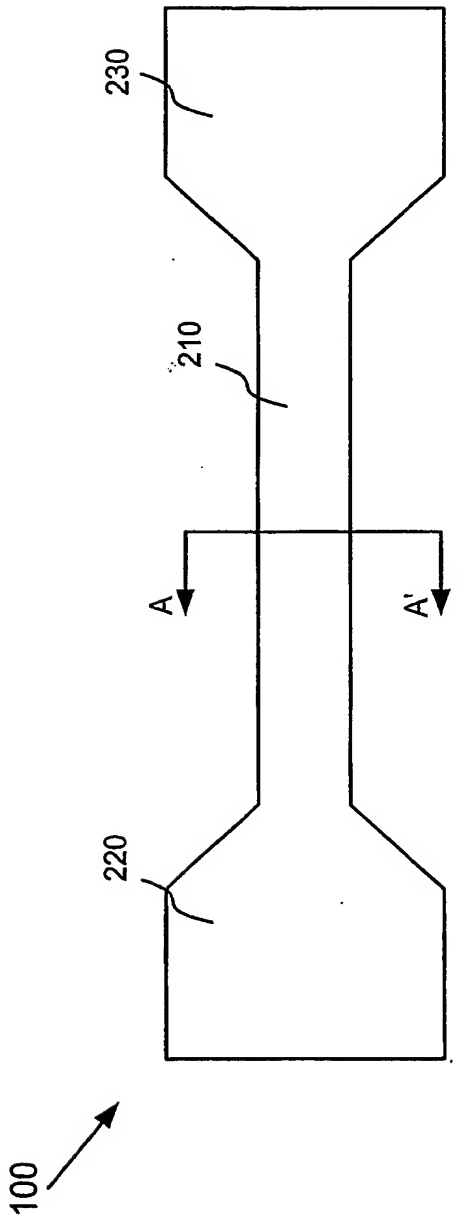
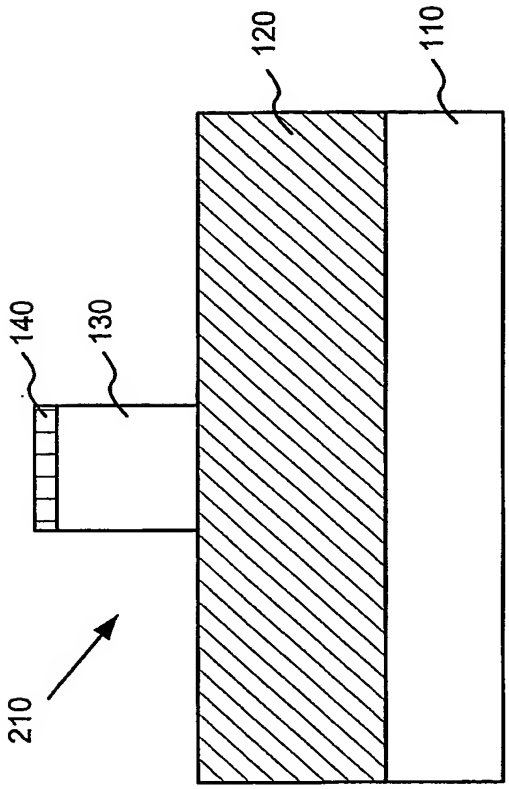


Fig. 2B



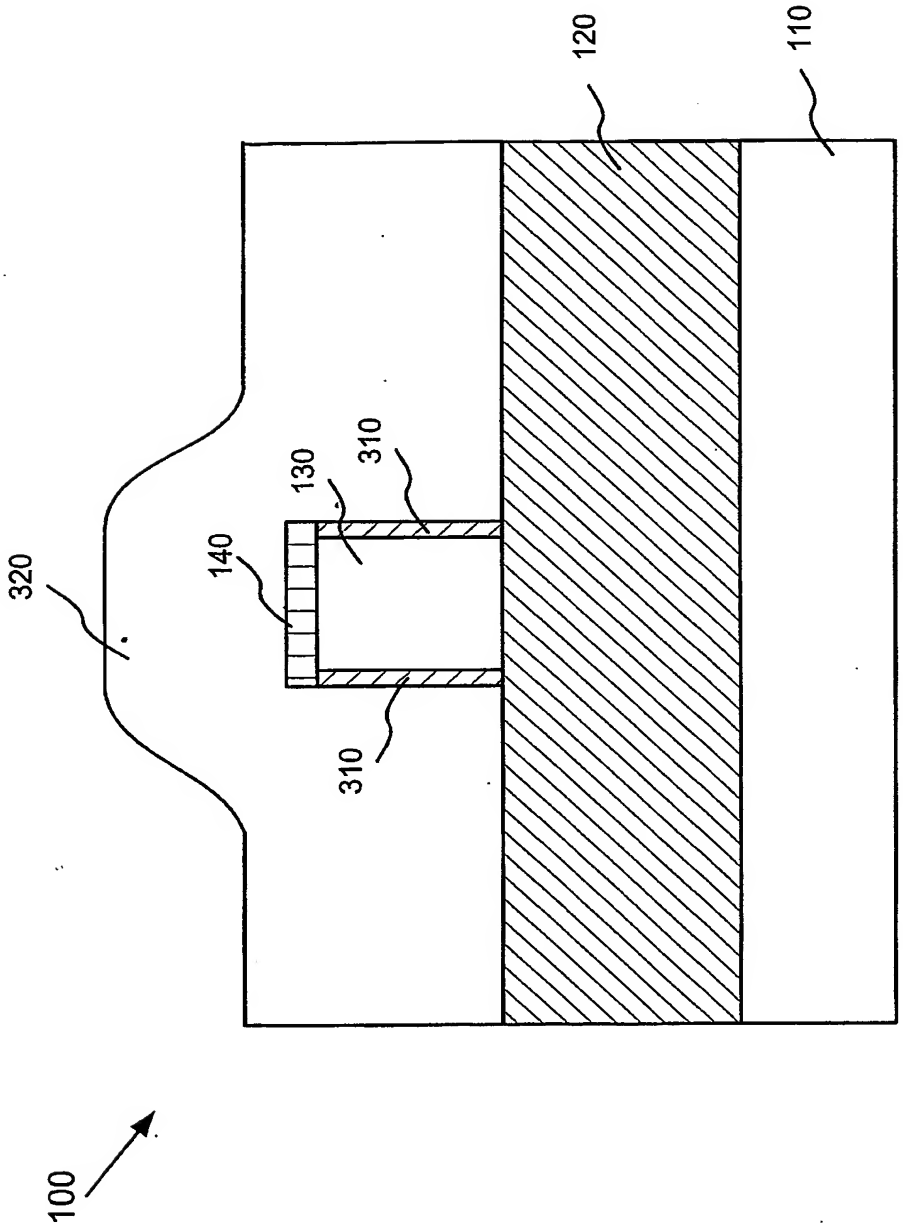


Fig. 3

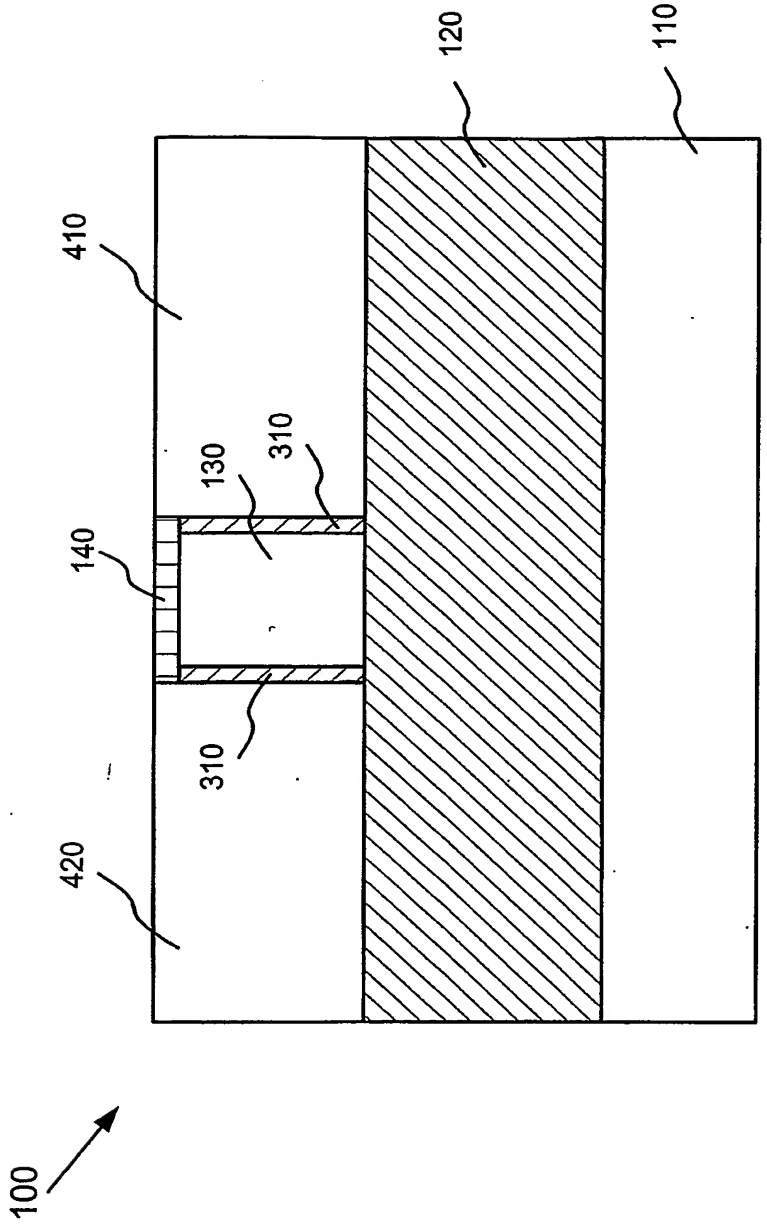


Fig. 4

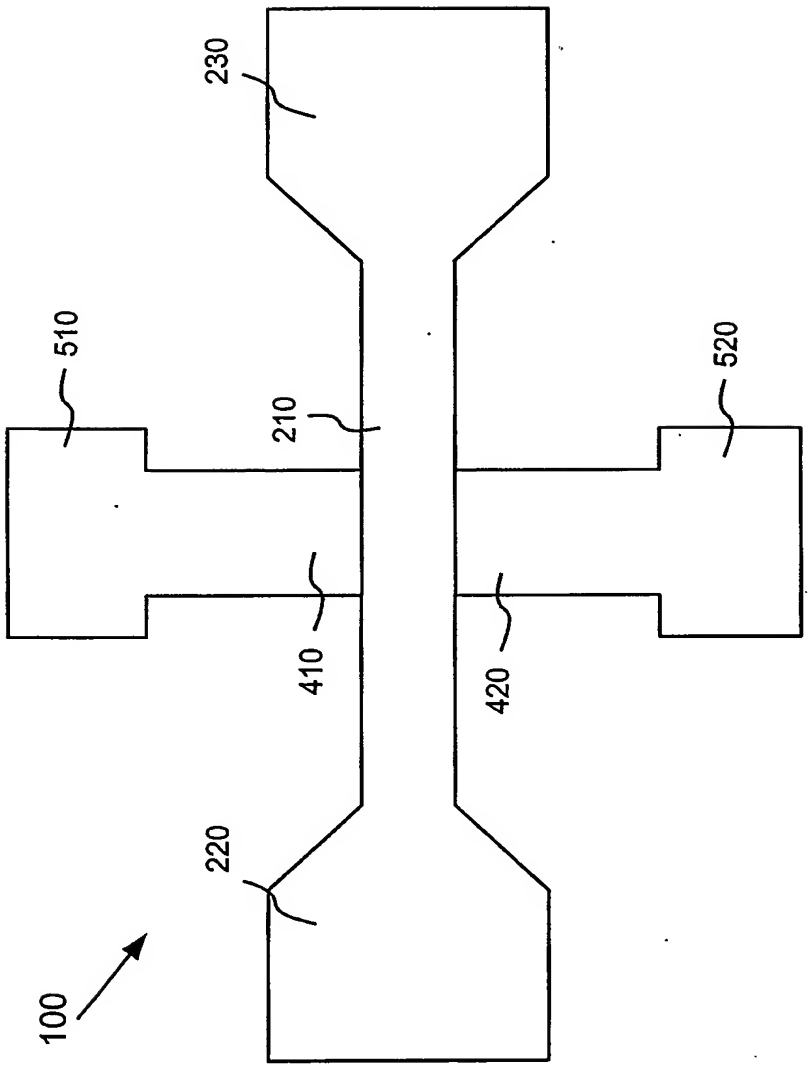


Fig. 5

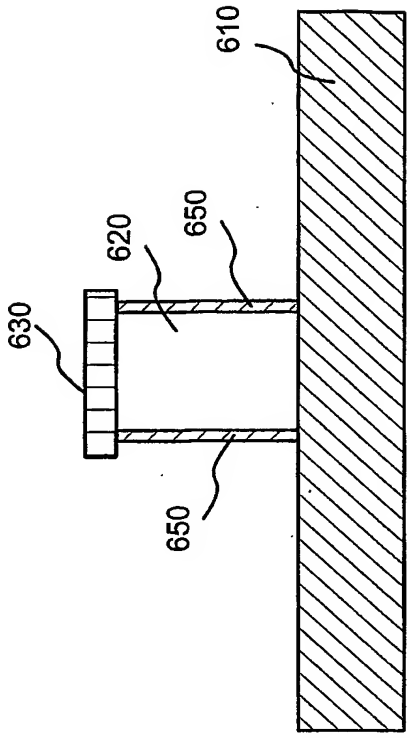


Fig. 6C

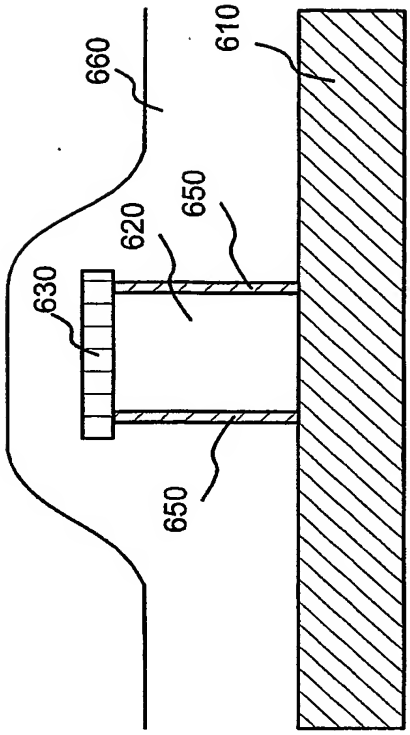


Fig. 6D

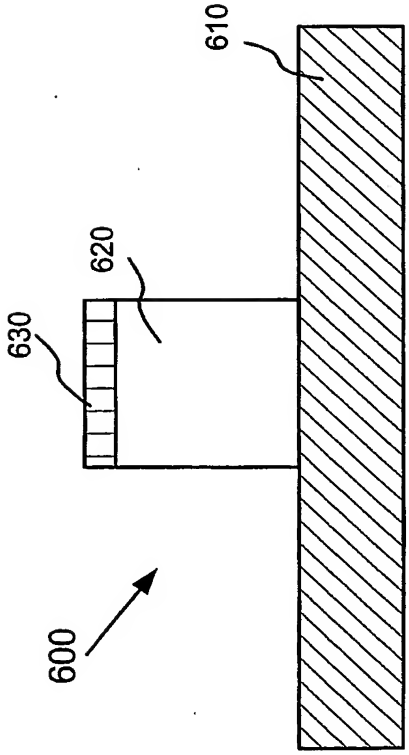


Fig. 6A

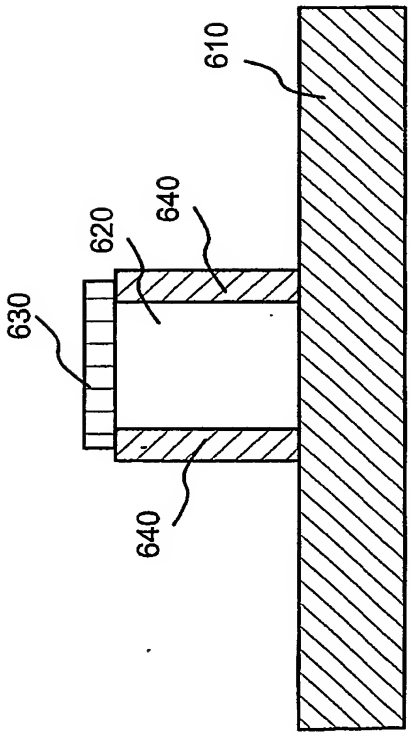


Fig. 6B

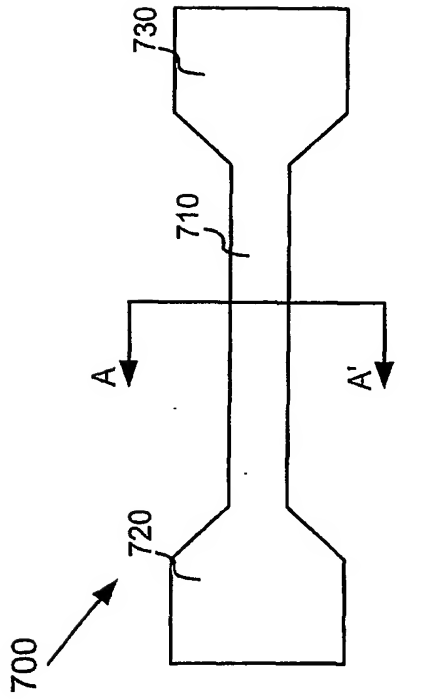


Fig. 7A

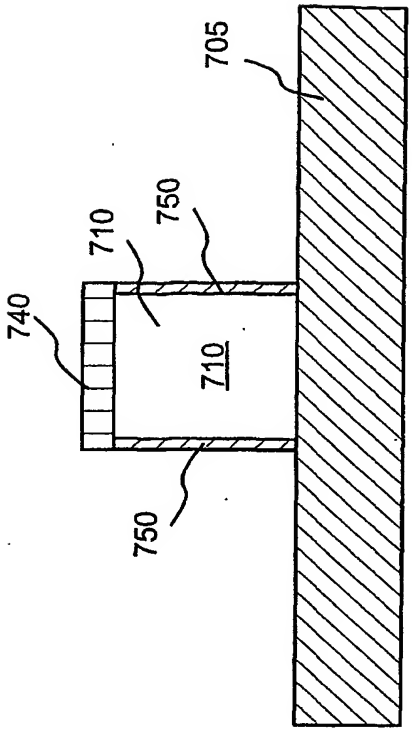


Fig. 7B

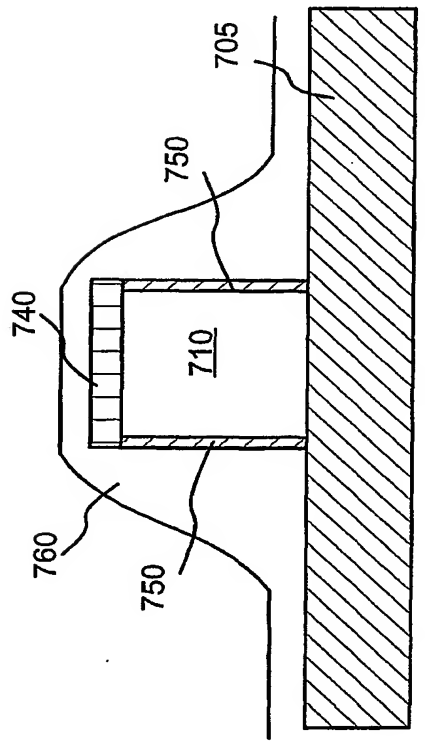


Fig. 7C

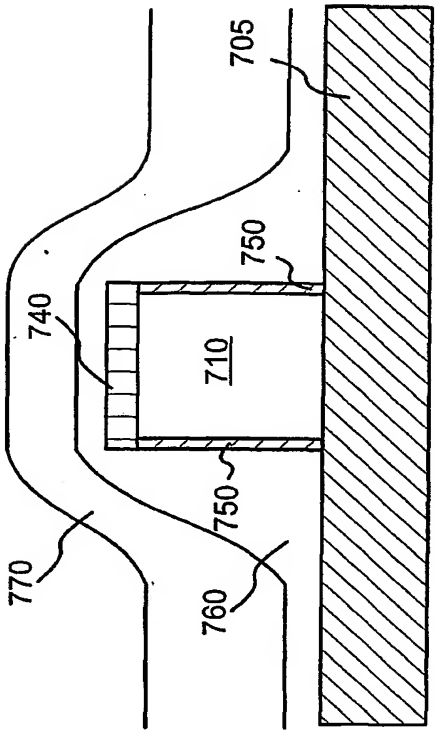


Fig. 7D

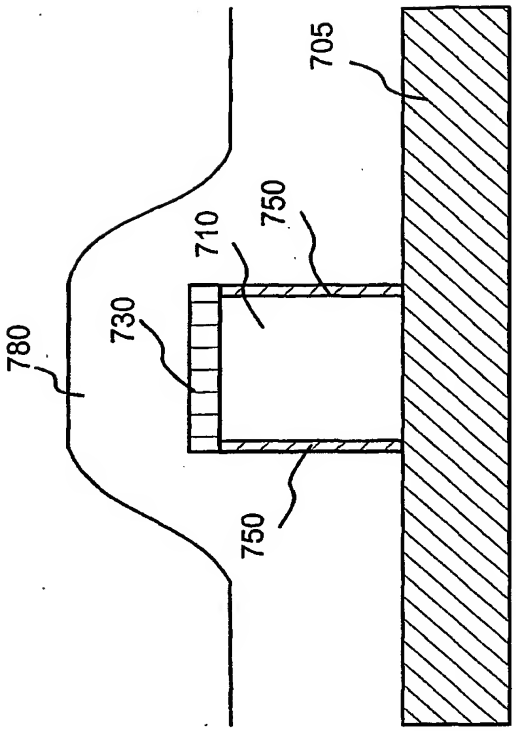


Fig. 7F

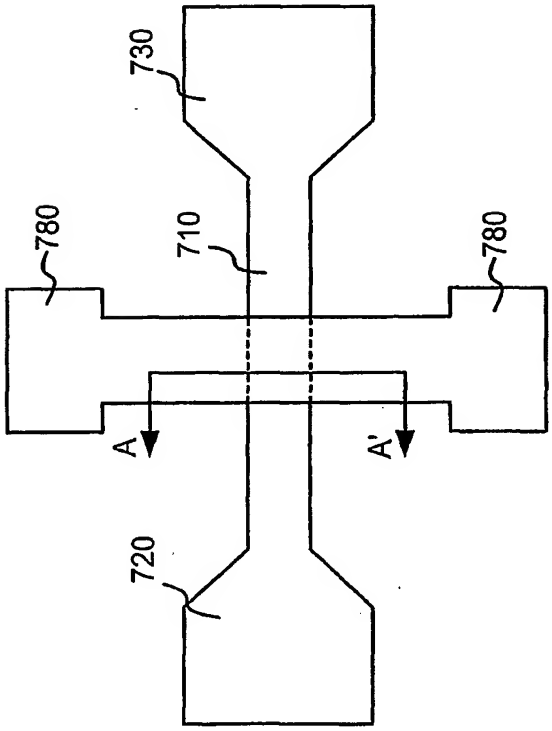


Fig. 7E

INTERNATIONAL SEARCH REPORT

Int ial Application No
PCT/US 03/32662

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/786 H01L29/423 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 563 082 A (MUKAI MIKIO) 8 October 1996 (1996-10-08) figures 5-7	1-10
X	US 5 315 143 A (TSUJI KAZUHIKO) 24 May 1994 (1994-05-24) figures 7B,7C	1-10
X	US 6 396 108 B1 (BUYNOSKI MATTHEW ET AL) 28 May 2002 (2002-05-28)	1-6,8-10
A	claim 1; figure 10	7

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 April 2004	21/04/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

Int[illegible]nal Application No
PCT/US 03/32662

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LELAND CHANG ET AL: "Gate length scaling and threshold voltage control of double-gate MOSFETs" IEDM, 10 December 2000 (2000-12-10), pages 719-722, XP010531863 figure 1	1-5,8-10
A	US 6 413 802 B1 (SUBRAMANIAN VIVEK ET AL) 2 July 2002 (2002-07-02) figures 1-6	5-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ial Application No
PCT/US 03/32662

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5563082 A	08-10-1996	JP 3252578 B2	04-02-2002
		JP 7193238 A	28-07-1995
US 5315143 A	24-05-1994	US 5409850 A	25-04-1995
		US 5541432 A	30-07-1996
		US 5565368 A	15-10-1996
US 6396108 B1	28-05-2002	NONE	
US 6413802 B1	02-07-2002	NONE	